REMARKS

The above-identified patent application has been reviewed in light of the Office Action dated December 20, 2001. In the amendments set forth above, Claims 7, 8 and 9 have been amended without abandoning or intending to dedicate to the public any patentable subject matter. Claims 1-6 have been withdrawn. Accordingly, Claims 7-12 are pending. For the reasons set forth below, the rejections of Claims 7-12 are respectfully traversed. Accordingly, reconsideration and withdrawal of the rejections of Claims 7-12 are respectfully requested.

Claim 9 stands rejected under 35 U.S.C. §112, second paragraph as being indefinite. In particular, the Office Action finds that the use of the phrase "desired characteristic" renders the claim indefinite. In the amendments set forth above, Claim 9 has been amended to replace the phrase "device characteristic" with the phrase "on current". In view of this amendment, it is submitted that the rejection of Claim 9 under 35 U.S.C. §112, second paragraph, should be reconsidered and withdrawn.

Claims 7-10 stand rejection under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,548,132 to Batra et al. ("Batra"). In order for a rejection under 35 U.S.C. §102 to be proper, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. (MPEP §2131). Claims 11 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Batra in view of the ordinary skill in the art. In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, there must be some suggestion or motivation to combine the reference teachings, there must be a reasonable probability of success, and the combination must teach or suggest all of the claim limitations. (MPEP §2143). As described more fully below, Applicants submit that Batra does not teach, suggest or

disclose a bottom gate thin film transistor in which the grain size of the source and the drain is greater than the grain size of the channel. Therefore, the rejection of Claims 7-12 should be reconsidered and withdrawn.

The claimed invention is generally directed to thin film transistors (TFT). In particular, a TFT in accordance with the now pending claims has a bottom gate structure and includes a polycrystalline silicon film in which a channel, a drain and a source are defined. Furthermore, the grain sizes of the drain and the source are greater than a grain size of the channel. (See Independent Claims 7 and 8).

Batra et al. is generally directed to a thin film transistor with a large grain size DRW offset region and small grain size source, drain and channel regions. (Batra, Title). In particular, Batra discusses a bottom gated thin film transistor that includes a drain offset region having a second average crystalline grain size larger than a first average crystalline grain size. The Office Action states that Batra in col. 5, lns. 10-59 discloses that the grain size of the source and drain region are larger than that of the channel region. However, the cited portion of Batra is directed to a top gated thin film transistor. (Batra, col. 4, lns. 58-59).

With respect to a bottom gated transistor, Batra discusses a drain offset region **66** having a second average crystalline grain size which is greater than the first average crystalline grain size of the remainder portion of thin film layer **60** (the source and drain regions **70, 72**). (Batra, col. 6, lns. 16-20). The drain offset region **66** is a portion of the drain region **70**. Accordingly, Batra et al. does teach, disclose or suggest a device in which the drain region (the drain offset region **66** and the drain region **70**) has a grain size that is greater than that of the channel region **62**. In addition, there is no discussion in Batra of a bottom gated TFT having a drain and a source with a grain size that is greater than the grain size of the channel, as required by the pending claims. Accordingly, the bottom-gated device discussed in Batra has drain, source and channel regions that all

feature a first average crystalline grain size, with only the drain offset region having a larger, second average crystalline grain size (Batra, col. 5, lns. 64-65 and col. 6, lns 11-20). Therefore, the pending claims are neither anticipated by nor obvious in view of the Batra.

Attached hereto is a marked up version of the changes made to the claims by the current amendment, captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is submitted that the application is now in form for allowance. Therefore, early notification of same is respectfully requested. The Examiner is invited to contact the undersigned by telephone if doing so would expedite the resolution of this case.

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Date: Jun 18, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend Claims 7, 8 and 9 as follows:

7. (Amended) A bottom gate thin film transistor comprising an active layer including a polycrystalline silicon film where a drain, a source and a channel are defined, grain sizes of the drain and source being [equal to or] greater than a grain size of the channel.

8. (Amended) A thin film transistor comprising:

an insulator substrate;

a gate electrode located on the insulator substrate;

an insulator film provided on the insulator substrate and the gate electrode; and

a polycrystalline silicon film located on the insulator film, a channel defined in a first portion of the polycrystalline silicon film over the gate electrode, a drain and a source defined in second and third portions of the polycrystalline silicon film over the insulator substrate, grain sizes of the drain and source being [equal to or] greater than a grain size of the channel.

9. (Amended) The thin film transistor according to claim 8, wherein the grain size of the channel is set large enough to provide a desired [device characteristic] on current of the thin film transistor.